of the communication bands. The asynchronous operation of these chirp filters with nominal processing gains of 30 dB and modest bandwidths exhibits exclusive advantages over the digital matched filter, with its inherent Doppler insensitivity, and should provide attractive compelling advantages in competing with present communication transmission techniques.

ACKNOWLEDGMENT

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A Review of Device Technology for Programmable Surface-Wave Filters

EDWARD J. STAPLES AND LEWIS T. CLAIBORNE

Invited Paper

***Abstract*—A review of programmable surface acoustic wave filters is presented. The elementary theory, fabrication procedures, and device performance are described in light of recent technological advances. Both hybrid and monolithic structures are considered. The relative advantages of programming techniques which utilize diode switching are compared to those that make use of solid-state, three-terminal, and acoustic wave detectors.**

I. INTRODUCTION

PRACTICAL surface acoustic wave devices are a reality for a variety of VHF and UHF filter and delay-line applications, e.g., bandpass filters [1], [2], pulse compression filters [3], and biphase coded matched filters [4]. The devices which have received the most attention and have been most extensively utilized for current systems hardware are based on Rayleigh wave propagation in piezoelectric substrates with fixed pattern interdigital transducers. For future systems needs [5]–[7], it will often be desirable to have available filters whose transfer functions are electronically programmable. It is the purpose of this paper to review the techniques which have been under development to provide surface-wave devices which can be programmed in real time for a variety of impulse responses.

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In its simplest form, the programmable surface-wave filter consists of a delay-line substrate which has a wide-band input transducer and a series of taps which are located at arbitrarily specified intervals down the propagation path. Parallel summation of the output from each tap forms a transversal filter [6] configuration, and in the general case, both the amplitude and phase of each tap are programmable variables. In this paper, we shall limit our discussion to surface-wave filters which have equispaced and constant amplitude taps, the programmable function being only the phase at each tap.

Most of the programmable filter development has been directed at biphase pseudonoise (PN) sequence matched filters for use in applications such as spread spectrum communications, ranging, and identification sequence generation and recognition [7]. The discussion in Sections II and III is concerned primarily with filter configurations which could be used in these applications.

The key component in all programmable filters is the acoustoelectric transducers used for signal taps. Methods of implementing diode-switched phase programming with the interdigital transducer on piezoelectric substrates are discussed in Section II; following this in Section III is a discussion of solid-state techniques for implementing other programmable transducers including the Si–metal–oxide–semiconductor field-effect transistor (MOSFET) and piezoelectric

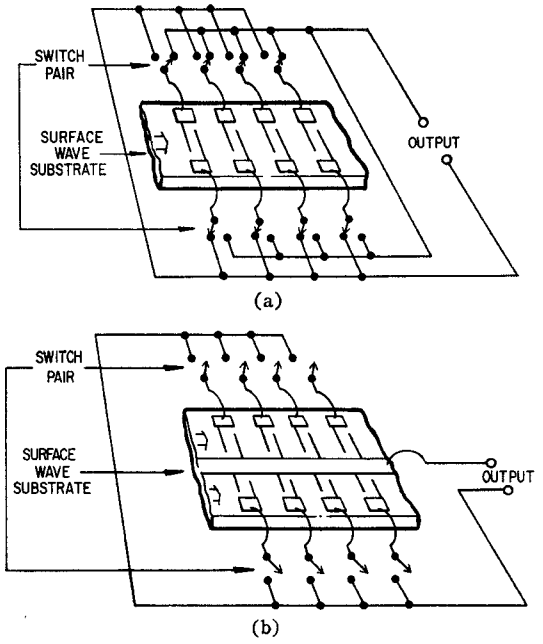

Fig. 1. (a) SPDT phase switching. (b) SPST on–off switching of surface-wave tapped delay line.

field-effect transistor. (FET). Also included in Section III is a discussion of a closely related monolithic technique using silicon on sapphire (SOS).

II. Diode Switching with Piezoelectric Tapped Delay Lines

Two basic types of RF switching are currently used with piezoelectric tapped delay lines. One approach reported [8] uses single-pole double-throw (SPDT) switches to control the phase of each tap as shown in Fig. 1(a). The delay line is particularly simple with this type of switch, i.e., it consists of N identical taps separated by a distance L corresponding to the chip rate [5] V_R/L, where V_R is the surface-wave velocity. The switches are operated in pairs with only one per pair in the grounded configuration at a time. The selection of one of the two possible switch states determines the phase of each tap. In a second arrangement shown in Fig. 1(b), a more complex dual acoustic beam delay line is required but the switch becomes a simple single-pole single-throw (SPST) type. In this technique, the phase of each tap is determined by switching on the transducer tap of appropriate phase. This latter approach is well suited to processing large chip counts in multiphased delay lines where the switching circuitry must be simple.

A. SPDT Diode Phase Switching

The phase of a piezoelectric tap may be switched $\pm 180°$ by the quad-diode arrangement shown in Fig. 2(a). The switch is activated by a switching voltage V_s applied through an isolation resistor R. With a positive voltage, diodes D_2 and D_3 are forward biased and exhibit a forward-biased resistance R_F. Diodes D_1 and D_4 are reverse biased and are represented by a reverse-biased capacitance C_R. A dc return path is indicated for diodes D_2 and D_4 that may be through the external load itself or provided by an RF choke in the output circuitry. Reversing the polarity of V_s has the effect of reversing the conduction states of the diodes and redirecting the tap output so as to reverse the phase of its contributions to the delay line output. Other more complex diode switch

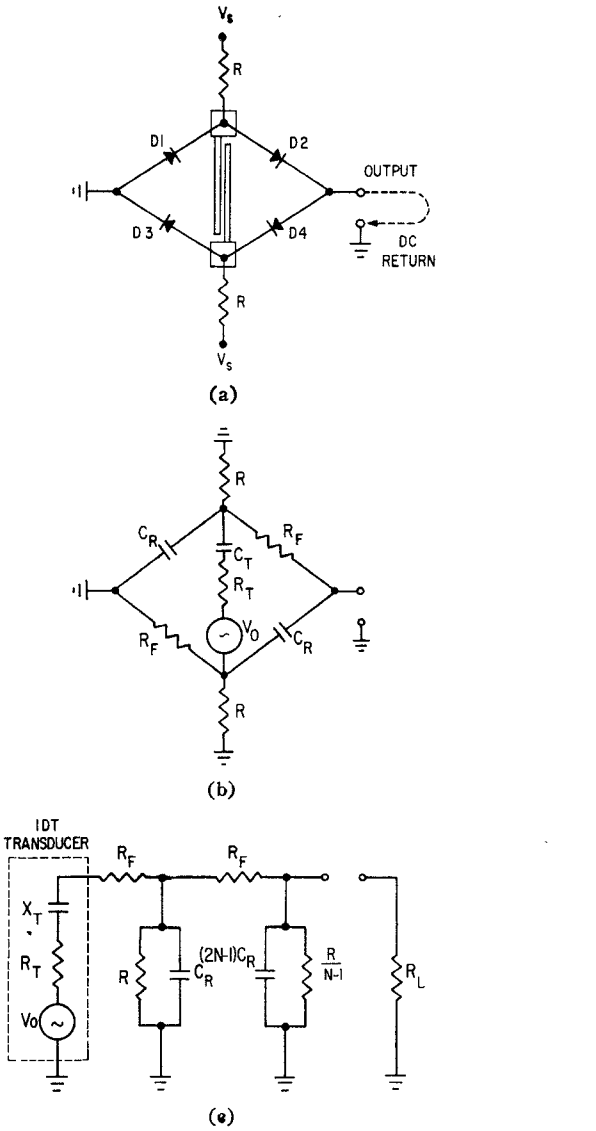

Fig. 2. (a) Quad-diode phase switch as applied to single tap. (b) Simplified equivalent circuit of transducer, switch, and 50-Ω output load.

circuits have been reported [9], [10]. However, the quad switch offers comparable performance with fewer components.

An exhaustive attempt will not be made to analyze the quad switch; however, some insight into its characteristics can be obtained by replacing each diode with its electrical equivalent, as shown in Fig. 2(b), for one polarity of V_s. The approximate equivalent circuit shown in Fig. 2(c) accurately represents the quad switch for $R \gg R_F$ and $R_F \ll 1/\omega C_R$, where R_F is the forward resistance and C_R is the reverse-bias capacitance of a single diode. The output load for the switch consists of a load resistance R_L (usually 50 Ω) in parallel with parasistic elements due to the other switching networks in a delay line with N taps.

For large N one finds that the presence of switch elements R, R_F, and C_R can seriously degrade the filter insertion loss. To examine this problem, let us consider the increase in tap insertion loss as the loading due to these elements becomes significant. The total insertion loss of the filter at the correlation peak will be assumed to degrade by the same amount. From the equivalent circuit of Fig. 2(c), two distinct effects can be seen to contribute to the insertion loss of a single tap.

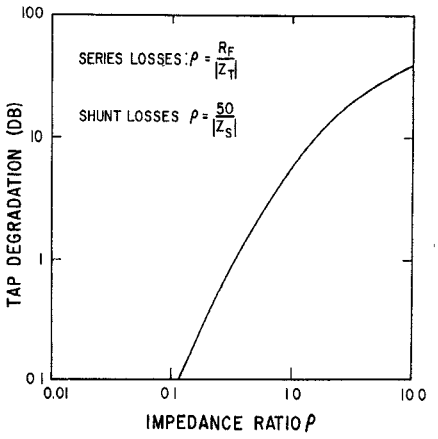

Fig. 3. Tap degradation in terms of series and shunt losses as a function of impedance ratio ρ.

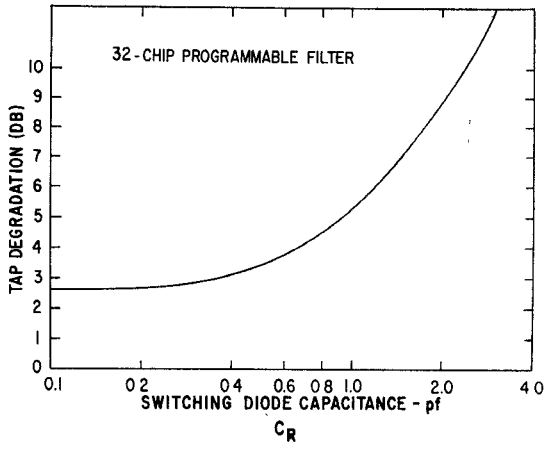

Fig. 4. Tap degradation as a function of reversed-biased diode capacitance for SPDT phase switching a 32-chip $LiNbO_3$ tapped delay line. $R_T = 100\ \Omega$, $C_T = 1.4$ pF, $f_0 = 60$ MHz, and $R_F = 10\ \Omega$.

The first is a shunting of the output due to the combined parasitic effects of all switching networks in parallel and represented by a shunting impedance Z_s. The second is due to series resistance R_F associated with the forward-biased diodes. Both effects are responsible for the net loss of the switch.

As a first-order approximation, each effect can be considered separately in terms of an impedance ratio ρ, where for series and shunt losses ρ is given by R_F/Z_T and R_L/Z_s, respectively, and Z_T is the transducer impedance. The tap degradation for each effect is then given in decibels by

$$20 \log \left| 1 + \rho \right|. \tag{1}$$

Shown in Fig. 3 is a plot of the loss associated with each type of effect as a function of ρ where Z_s and Z_T are assumed to be purely capacitive reactances. For most delay line taps, only a small number of finger pairs are used and Z_T is a relatively large capacitive reactance.

The biasing resistors and reversed-biased switching diodes contribute the shunting impedance of the diode switch. Since the N taps are connected in parallel, the reactance or impedance can become a problem. For example, if $|Z_s| < R_L$, the degradation is greater than 6 dB. Although the biasing resistors can be replaced with suitably chosen inductors, the reverse-biased diode capacitances still can be a problem when devices with many taps are considered. Fig. 4 shows theoretically the effect of diode capacitance for a 32-chip $LiNbO_3$ programmable filter. In this case, 4000-Ω bias resistors were used and contributed the majority of the 2.5-dB degradation loss present with no reversed-diode capacitance. The reverse-biased capacitance of the switching diodes is seen to contribute little effect until values greater than 0.6 pF are exceeded. For the same 32-chip delay line, the tap impedance and diode forward resistance were typically 2000 Ω and 10 Ω, respectively. From Fig. 3, the series losses accounted for less than 0.1 dB. In fact, a forward resistance of 200 Ω would have only degraded the output 0.8 dB. Thus for the SPDT switch, shunting losses account for the majority of the tap degradation. In order to maintain low insertion loss as the frequency or the number of taps of the delay line are increased, the reverse-biased capacitance must also be decreased. The parallel summation of the switch parasitics appears to be the primary limitation for this type of switch.

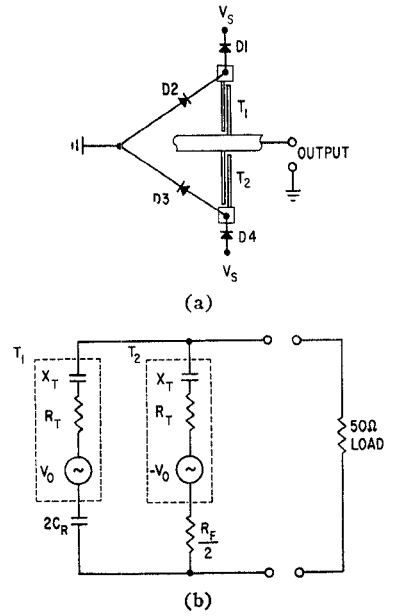

Fig. 5. (a) Diode arrangement for SPST on–off switching a single two-transducer tap. (b) Simplified equivalent circuit of transducers and switch coupled to 50-Ω load.

B. SPST Diode Switching

The SPST RF switching scheme utilizes a dual acoustic beam delay line for phase reversal as shown in Fig. 1(b). This configuration has the relatively simpler switching network illustrated in Fig. 5(a) for a single tap. A positive switching voltage turns D_3 and D_4 on, and a negative voltage turns D_1 and D_2 on, resulting in one of the two transducers of differing phase being connected to the output sum line. The equivalent circuit for one tap is shown in Fig. 5(b), where the transducers T_1 and T_2 are shown as voltage sources of opposing phase. There is one obvious advantage to this type of switch; all parasitic switch capacitances are in series with the transducer and are not connected in parallel with the sum line. This implies the extension to a large number of taps without parasitic buildup. However, the requirements placed on the diodes are much more stringent than in the case of SPDT switching. For this type of switch, the on–off ratio is a measure of the switch performance. The ability to turn off the tap influences the insertion loss strongly.

For the condition $(R_T)^2 \ll X_T^2$, the insertion loss into 50 Ω can be shown to be proportional to $(X_T)^2$. When one side of the tap is off, its signal will drop by $-10 \log (1 + C_R/C_T)^2$ in

accordance with simple voltage division. For most tapped delay lines, the transducer tap capacitance C_T is typically 1 pF or less. Hence, it would not be unreasonable to expect the diode capacitance to be equal to the transducer capacitance. In this case, half the voltage is reactively canceled and the total tap insertion loss is degraded -6 dB from the loss without the switch. However, in some circumstances, this can be improved by designing the tap and substrate combination to have a large capacitance, i.e., using more finger pairs on such materials as $LiNbO_3$. Furthermore, the ability to generalize to N taps without additional buildup of parasitics due to additional switches and the simple switch design itself is a compelling motivation for SPST switching.

Because of the need for isolation, switching circuitry must be fabricated on insulating substrates and can be made using thin-film techniques [11]. However, to achieve bit rates above 10 MHz, the switching circuitry rapidly goes beyond current linewidths achievable with thin-film fabrication techniques. Furthermore, the use of wire bonds between switching circuitry and delay line can become a problem as the frequency is raised [12], in terms of reliability [13]. The fabrication of switching diodes using SOS techniques can be used to obtain higher density. However, the interconnection problem remains and necessitates an integrated monolithic approach.

III. Solid-State Programmable Filters

Solid-state detectors are a combination of detector and switching resulting in a three-terminal active device, whereas the IDT is a two-terminal passive device. These types of detectors utilize the self-isolation of the third terminal to simplify switching functions without the normal RF parasitic reactances. The main difference between solid state of detectors and the previously described IDT structures is in the detectors themselves. By using solid-state devices for the detection of the surface waves, the number of bonds required is greatly reduced. In addition, the reliability is increased, higher bit rates are made available, and the cross talk is reduced. Furthermore, the use of semiconducting substrates for both the surface wave and switch circuitry enables the fabrication of a monolithic structure with a minimum of external connections.

Three types of solid-state detectors will be considered here. First in our discussion is the Si–MOSFET that makes use of the piezoresistance effect due to an interaction between the surface wave and electrons (or holes) flowing in an inversion layer [14], [15]. Second is the piezoelectric FET which utilizes a piezoelectric interaction to detect the surface wave. The GaAs FET has been reported [16] for the detection of surface waves as well as a closely related Si–MOSFET with a piezoelectric gate oxide [17] instead of SiO_2. Finally, a discussion of the integration of acoustic and electronic technologies on a common sapphire substrate will be considered.

A. Si-MOSFET

The piezoresistance effect in Si–MOSFET inversion layers has been used for the detection of elastic surface waves [15]. The piezoresistance effect is a result of the modulation of the effective carrier mobility by an applied stress. This modulation arises from the nonspherical nature of the Fermi surface in multivalleyed semiconductors. The phenomenological relations between electric field, current, and stress can be written for the major crystallographic directions of a material as follows:

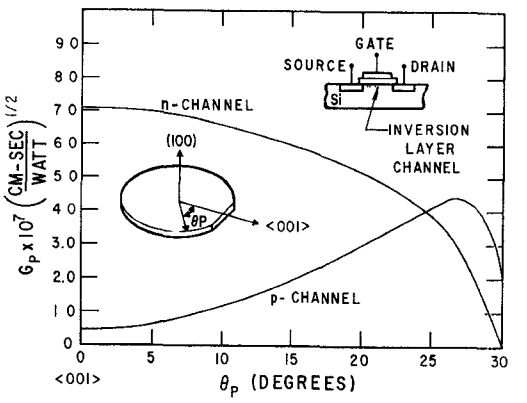

Fig. 6. Normalized gauge factor for surface-wave modulation of n- and p-type MOSFET's on the (100) plane of silicon as a function of propagation direction. Current flow is in direction of propagation θ_p.

TABLE I
Single MOSFET Detection Characteristics

Type	Orientation	Gauge Factor[a]	Insertion Loss (dB)[b]
p	(100), 0°, ⟨001⟩	0.4×10^{-7}	~70
p	(100), 25.5°	4.0×10^{-7}	58
p	(110), 0°, ⟨$\bar{1}$10⟩	4.5×10^{-7}	57
p	(110), 55°	3.0×10^{-7}	62
p	(111), 0°, ⟨$\bar{1}$10⟩	2.5×10^{-7}	64
p	(111), 30°	3.1×10^{-7}	61
n	(100), 0°, ⟨001⟩	7.1×10^{-7}	51
n	(100), 25°	4.0×10^{-7}	58

[a] Units: $(cm\cdot s/W)^{1/2}$.
[b] $I_{dc} = 50$-mA unmatched 50-Ω load.

$$\sigma_{ij}E_{ij} = I_i + \pi_{ijkl}I_jT_{kl} \tag{2}$$

where σ_{ij} is the conductivity tensor and π_{ijkl} is the piezoresistance tensor. The piezoresistance effect in both p- and n-channel inversion layers in silicon has been described by a two-dimensional piezoresistance tensor for a stress-free surface [14].

To describe the modulation of the drain current in an Si–MOSFET due to a surface wave, it is necessary to calculate the stresses associated with wave propagation for a specific crystal plane and wave vector direction θ. The dc current components $I_i(\phi)$ are determined by the magnitude of the dc current and the MOSFET orientation ϕ on the crystal plane. Using the piezoresistance tensor relation (1), an equation can be derived for the RF current modulation i at a frequency ω for an arbitrary wave vector and current direction, i.e.,

$$i = G(\theta, \phi)\sqrt{(\omega/W)P_a(\theta)} \tag{3}$$

where $P_a(\theta)/W$ is the acoustic power per unit width.

The gauge function $G(\theta, \phi)$ is normalized to surface-wave acoustic power $P_a(\theta)$ and has the dimensions of $(cm\cdot s/W)^{1/2}$. A detailed analysis of $G(\theta, \phi)$ for both p- and n-channel MOSFET's on most of the major crystal planes of silicon has appeared earlier [18], [19]. Gauge factors for both n- and p-channel MOSFET's are shown in Fig. 6 for the (100) plane of silicon. The results of these investigations have shown n-channel MOSFET's to have the largest gauge factors and p-channel MOSFET's to be somewhat lower. Shown in Table I are some typical gauge factors for both p- and n-channel MOSFET's in selected orientations.

Although the gauge factor is a measure of the detection efficiency, also shown in Table I are the insertion losses

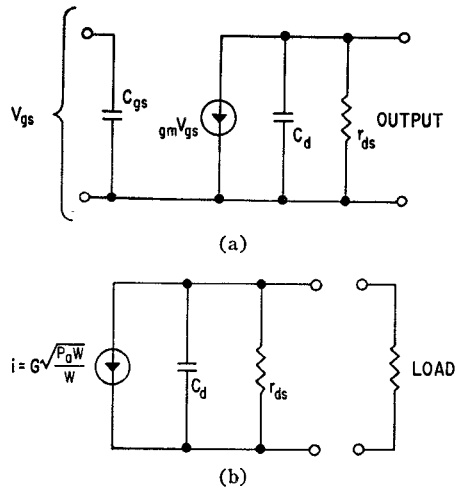

Fig. 7. (a) MOSFET simple equivalent circuit. (b) Equivalent circuit applicable to surface-wave drain current modulation.

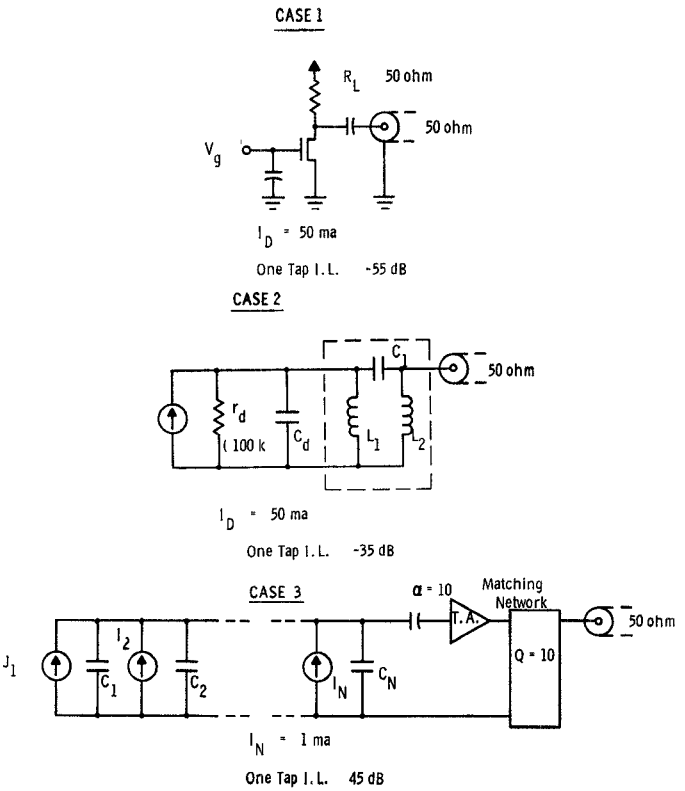

Fig. 8. MOSFET insertion loss characteristics for three cases of loading. Case 1 is unmatched, Case 2 represents passive matching, and Case 3 involves active matching and a MOSFET tapped delay line.

associated with piezoresistive MOSFET detectors at a bias current of 50 mA and with a 50-Ω load. At this point, a word of caution should be given regarding the insertion loss of active (electronically) surface-wave detectors. Unlike piezoelectric IDT structures, these devices are characterized by equivalent circuits whose components are independent of acoustic properties. In this case, insertion loss is a function of both acoustic and electronic properties, and care must be taken to select proper electrical loading such that electronic and acoustic efficiencies can be analyzed separately. The MOSFET is such a device and has the simplified equivalent circuit of Fig. 7(a). When used as a programmable surface-wave detector, the gate is at RF ground and merely switches the drain current on and off with a dc voltage. In this case, the simple circuit of Fig. 7(b) results. The strength of the current source is given by (2). However, the drain-to-source conductance $1/r_{ds}$ and capacitance C_{ds} are independent of acoustic excitation. The drain-to-source capacitance is merely that associated with the reverse-biased drain diode and can be very small. The conductance $1/r_{ds}$ has been analyzed for many types of MOSFET structures [20] and is typically 10 kΩ or greater, depending upon biasing conditions. By loading the output with 50 Ω, the MOSFET current source is effectively shorted and a meaningful evaluation of the acoustic modulation can be made. However, if one considers the insertion loss under matched conditions, i.e., $R_{load} = r_{ds}$, the insertion loss improves by 10 log $(r_{ds}/50)$, which can be substantial. Insertion losses as low as −35 dB have been obtained with a single tap; however, this is more a function of matching network rather than MOSFET acoustic properties. Thus the complete coupling circuit between tap and load must be considered to interpret the total device insertion loss.

Assuming a constant frequency and acoustic power density, the preceding comments regarding insertion loss are illustrated by the three cases shown in Fig. 8. Case 1 is that of a single unmatched MOSFET with a drain current of 50 mA resulting in typically −55 dB insertion loss. Case 2 represents the equivalent circuit (drain only) of the same MOSFET terminated with a matching network resulting in a 20-dB improvement. However, the amount of improvement is proportional to the Q of the matching network and is obtained at the expense of reduced bandwidth. Case 3 illustrates an approach applicable to a MOSFET programmable tapped delay time where N MOSFET's are shown as N current sources shunted by N drain capacitors. The effects of the shunting reactances are virtually eliminated by operating into a transimpedance amplifier (TA) with a current gain of 10. This also enables a reduction in drain current without an increase in insertion loss. The insertion loss is further improved by a matching network with a Q of 10 resulting in a total per tap insertion loss of −45 dB.

The ability of the MOSFET (as well as other FET structures) to operate well into the gigahertz frequency range [21] is only of secondary importance since the frequency response of any surface-wave detector is governed by the size of the active channel length L relative to the acoustic wavenumber $\beta = 2\pi/\lambda$, resulting in a $(\sin(\beta L/2)/\beta L/2)^2$ response. The ability to fabricate MOSFET's with micron channel lengths has been demonstrated [22]; hence, the acoustic frequency response of the detectors will not degrade until the acoustic wavelength approaches these dimensions.

Illustrated in Fig. 9 are the three important building blocks of a MOSFET programmable filter. In the top left block is the input transducer consisting of a deposited (piezoelectric) ZnO film and overlayed interdigital electrodes. The ZnO overlay transducer [23] has received considerable attention and represents a planar structure compatible with silicon processing for generating acoustic surface waves in nonpiezoelectric substrates. In the top right block is the MOSFET delay line where each tap consists of a staggered pair of MOSFET's such that their outputs are 180° out of phase at the center frequency of 70 MHz. Since the piezoresistance effect is proportional to the surface-wave amplitude and not to the total power in the substrate, the insertion loss is independent of its physical size within a straight crested wavefront. Hence, no loss is incurred by reducing the size of the detectors. In the final block is a static MOS 10-chip shift

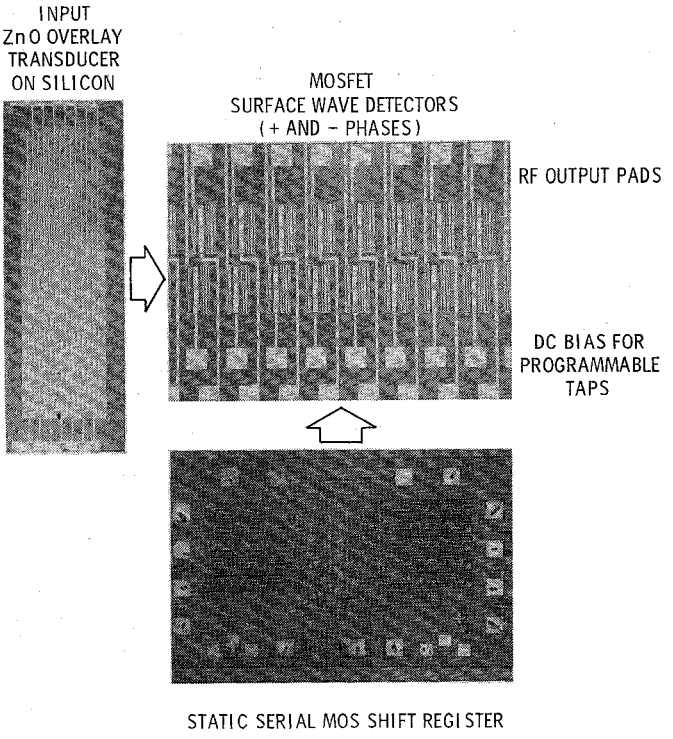

Fig. 9. Basic building blocks for MOS programmable filter.

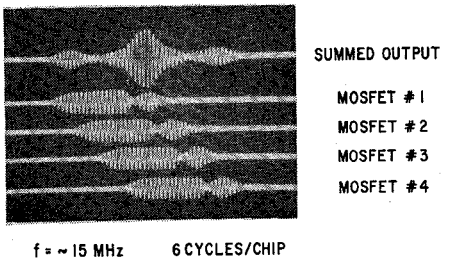

Fig. 10. Summed output from a MOSFET tapped delay line showing correlation of simple 4-chip sequence.

register (TI number TMS-3007) with serial input and parallel output to drive the MOSFET detector array gates. All of the blocks are compatible with standard MOS processing and represent one approach to the implementation of a monolithic programmable filter. Since the output of an array is proportional to either the current or number of taps squared, the total insertion loss can now be estimated by considering the loss of a single MOSFET but operating with the total array drain current.

The actual insertion loss will be the single-tap total-current loss plus any code and/or mismatch losses. In effect, the total array current is spread over the individual MOSFET's and recombined in the correlation output. A simple demonstration of the correlation properties of a MOSFET tapped delay line is shown in Fig. 10. The correlation of a simple biphase coded 4-chip Baker sequence at 15 MHz is shown in the upper trace and is the sum of the four individual MOSFET outputs shown below it where the proper phase and time delay of each tap was determined by the physical placement of the MOSFET's within the acoustic beam.

B. Piezoelectric FET's

In some cases, lower insertion loss per tap can be obtained using a piezoelectric rather than a piezoresistive FET to detect surface elastic waves. Two types of piezoelectric FET's have been reported for the detection of surface waves, although a rather large family of stress-detecting FET's exist [24]. Representative of one type of three-terminal piezoelectric detector is the GaAs FET shown in Fig. 11. The surface wave propagates on a layered substrate comprising an epitaxially deposited thin layer of GaAs on a semi-insulating GaAs substrate. Electronic conduction between the source and drain ohmic contacts is controlled by the depletion region of the Schottky barrier gate electrode. The gate may be used to launch and receive acoustic surface waves, although lower conversion loss is obtained by taking the received signal out of the drain rather than the gate contact [16], [25]. Tuned conversion losses as low as −26 dB have been obtained with this type of FET; however, the coupling phenomena is somewhat complicated by the presence of two interactions taking place within the FET. The surface wave can modulate the source–drain current by 1) inducing an RF voltage on the gate which is then amplified by normal transistor action, and 2) producing a carrier-density modulation via the piezoelectric interaction with drifting carriers in the FET channel. Both effects have been observed [25], and analysis is further complicated by the complexity of both the electric field of the FET and the surface elastic wave.

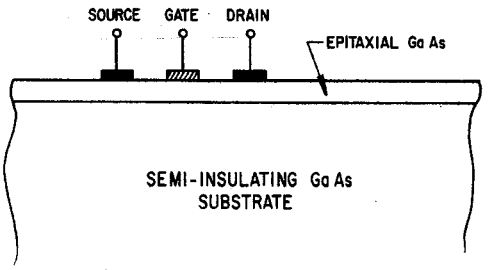

Fig. 11. Piezoelectric GaAs FET structure used to detect surface waves. Current between source and drain is controlled by Schottky barrier gate electrode.

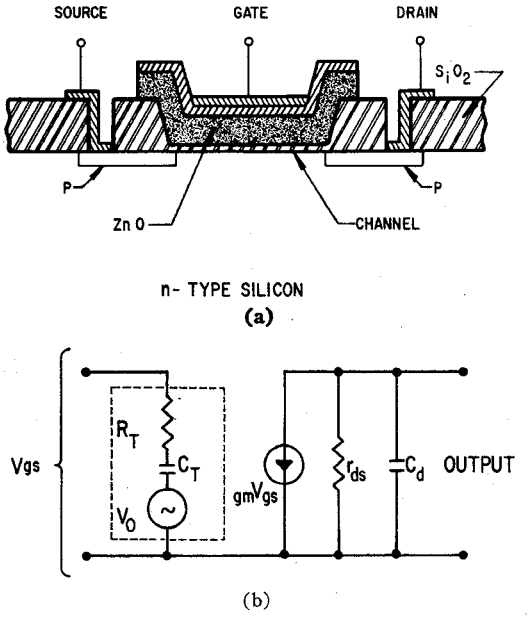

Fig. 12. (a) Cross section of piezoelectric MOSFET with ZnO gate. (b) Modified equivalent circuit with piezoelectric gate input.

A second type of piezoelectric FET which has been used to detect surface waves [17] is shown in Fig. 12(a). The

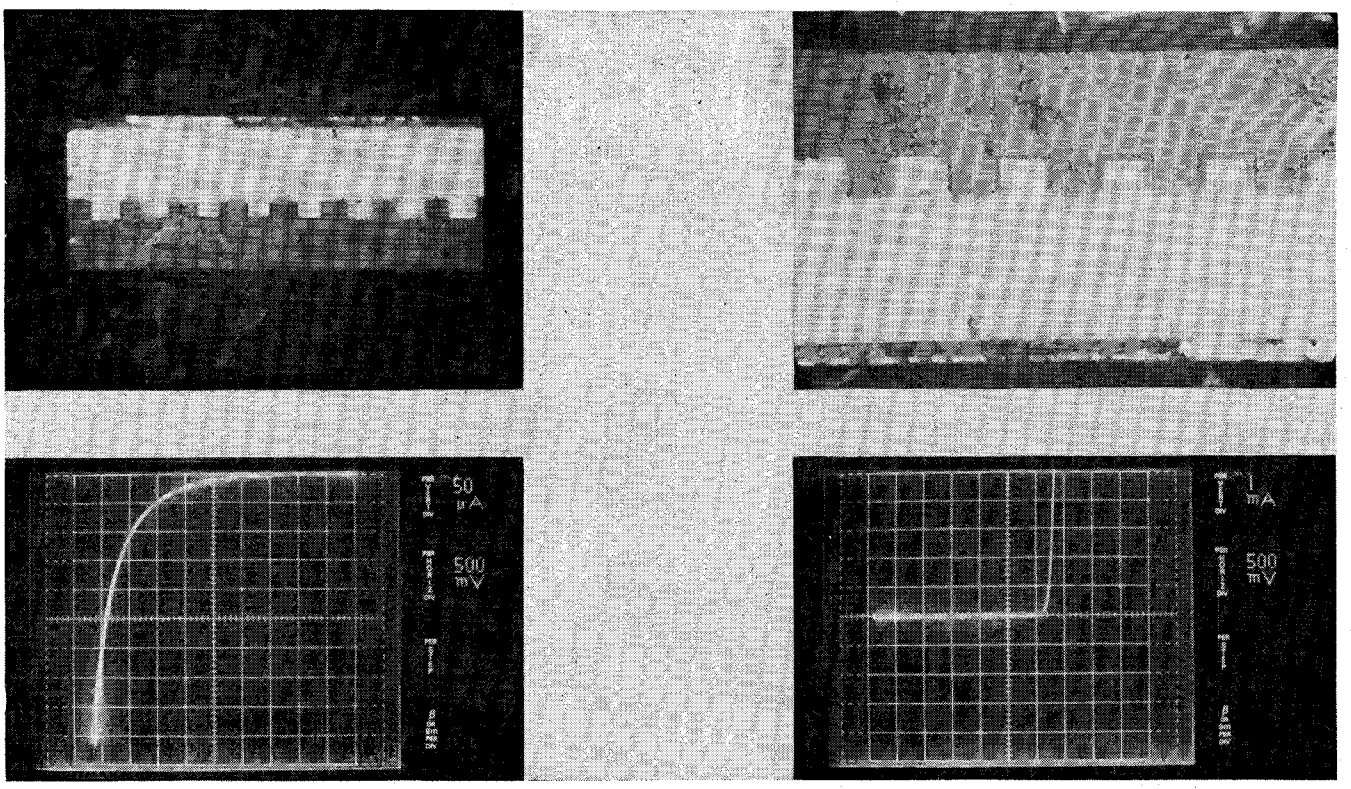

Fig. 13. SOS diode switching elements and their I–V characteristics.

structure is basically a MOSFET with a piezoelectric oxide (i.e., ZnO) as the gate oxide. This differs from the GaAs FET due to a separation of the piezoelectric medium from the semiconductor region, and this allows separate optimization of free-carrier transport properties and of the piezoelectric properties. Due to the extended depletion region surrounding the MOSFET structure, that type of coupling whereby the source–drain current is modulated by charge carrier-density effects will be reduced. In this case, one approach has been to assume the generation of a polarization voltage by a surface wave. The strength of this voltage can be related to the coupling factor which has been done for such materials as ZnO and CdS [23]. In effect, the gate electrode becomes a single interaction in a grating mode overlay transducer. The equivalent circuit in this rather simplified case is shown in Fig. 12(b).

Silicon-based, piezoelectric or piezoresistive, FET's, bipolar's, and particularly MOSFET's, are attractive for programmable filters in view of their well-established shift register and memory capabilities. A completely monolithic batch-processed relatively inexpensive programmable matched filter will result in the minimization of bonds to the level of a common 16-p-i-n package.

C. SOS Programmable Filters

Epitaxially deposited SOS as a substrate for the fabrication of diodes and transistors promises to innovate these conventionally silicon-based devices. Recent advances in the techniques of material growth, fabrication procedures, and device performance have been reported. [26] From an electronic point of view, the attractiveness of the SOS approach stems from the fact that by being on an insulator there is no parasitic capacitance between the active circuit and the substrate. As noted earlier, in connection with diode switching of piezoelectric delay lines, either SPDT or SPST, a limiting design factor was the capacitance associated with the reversed-biased diodes themselves. In addition to reducing substrate capacitance, the SOS approach leads directly to complementary integrated circuitry since all that is required is a simple removal (etch) of the excess silicon surrounding each active device. Thus every device is completely isolated from other circuit components regardless of its particular type (n- or p-type). Both of the aforementioned characteristics of the SOS approach make it well suited for implementation of programmable filters utilizing either diode switched IDT's or active FET detectors.

To date, the SOS approach has only been reported for diode switching of piezoelectric delay lines. Initial efforts [12] utilized the SOS diodes shown in Fig. 13. The diodes were fabricated in a 1.7-μm-thick silicon film deposited on a sapphire substrate. The silicon was etched into arrays of eight p^+-n^+ diodes, 8 mil wide, and the whole structure metallized with 1 μm of aluminum. The resulting diodes had a reverse breakdown (Zener) of -4 V, a forward resistance of 7 Ω, and an interelectrode capacitance of approximately 0.5 pF. The diodes were then bonded to an IDT delay line ($LiNbO_3$), as shown in Fig. 14. The resulting 16-chip programmable tapped delay line operated at 60 MHz, with a 5-MHz chip rate. Also shown are the input–output waveforms for a single 16-chip sequence.

The preceding programmable filter demonstrates the ability of SOS diodes to switch IDT tapped delay lines; however, it also clearly shows the large number of bonding wires required for a programmable filter in hybrid form. As the frequency or number of taps is increased, the parasitic effects of the bonding wires becomes the main motivation for a monolithic structure consisting of delay line and switching circuitry on the same sapphire substrate.

Fortunately, the excellent epitaxial characteristics of sapphire have been demonstrated for several piezoelectric films

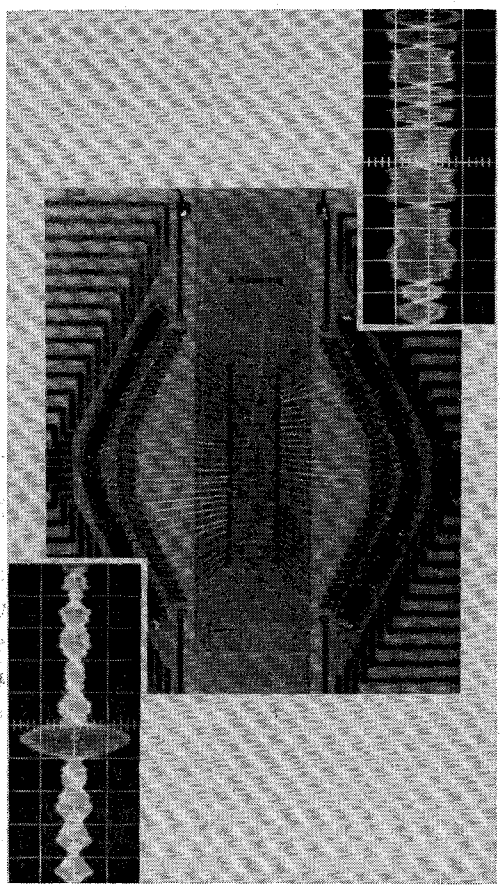

Fig. 14. Biphase coded 16-chip programmable filter with input–output waveforms (time scale: 0.32 μs/div.)

[27], [28], thus providing the required IDT substrate. In addition, sapphire as a surface-wave substrate is attractive because of its relatively high velocity (~6000 m/s) and low acoustic attenuation. Thus the requirements for a monolithic programmable filter can indeed be met by the SOS approach for switching circuitry and piezoelectric film deposition for delay-line construction.

In principle, the design and fabrication of a monolithic sapphire-based programmable filter merely involves a combination of two established technologies. However, as with most such integrations, this can be misleading. Initial efforts [29] toward such a device utilized SOS diode logic and switching circuitry with an epitaxially grown ZnO film for the surface-wave medium. Problems were experienced with the ZnO and the diode logic. Since ZnO is a slow material (V ~2700 m/s) compared to sapphire, dispersion in the acoustic delay line could only be avoided by using a thick ZnO film. This is turn created problems with the subsequent contact photomasking since the ZnO film prevented contact between the mask and substrate. In addition, the ZnO was not compatible with subsequent high-temperature SOS processing steps and required polishing to reduce surface roughness and hence acoustic attenuation. These problems were compounded by the inability of the diode logic to drive the switching networks due to an excessively high sheet resistance in the silicon interconnect lines.

These problems led to a second design [30], [31] utilizing MOS shift-register logic circuitry to drive SOS diode switches and AlN as the piezoelectric film on sapphire. The acoustic velocity in AlN closely matches that in sapphire; hence, dispersion is reduced as well as required film thickness. This has the effect of reducing acoustic attenuation and eliminating the previous photomask contact problems. The MOS logic utilizes p-channel MOSFET's to switch the bias voltage on the diode–bridge tap switches described previously. Since these transistors are used as a direct link to the bias supplies through metal interconnections and are switched by their high impedance gates, the need for low sheet resistance in the SOS circuitry is eliminated.

IV. Summary

One goal of this paper has been to review those efforts that are being made toward the integration of acoustic and electronic technologies for programmable matched filters.

Initial efforts in realizing a programmable filter used hybrid integration involving diode-switching networks applied to the taps of a surface-wave tapped delay line. The resistive, on–off ratio, and shunting losses of phase (SPDT) and amplitude (SPST) switching networks were described in terms of simple equivalent circuits. The tap degradation for the phase switch is proportional to both frequency and chip-sequence length because the shunting losses in each tap switch are in parallel. Conversely, amplitude switching has a somewhat larger initial tap degradation which is not a function of either frequency or chip-sequence length. All diode characteristics being considered equal, the phase switch offers the lowest tap degradation for small to medium chip-sequence lengths and frequencies below 100 MHz. However, in general, the choice of whether to use phase or amplitude switching will be determined by the particular application.

The performance of hybrid integration techniques for programmable surface-wave filters with chip rates in excess of 10 MHz and chip-sequence lengths greater than 100 is questionable due to the large number of bonds required within the space available. In addition, the large number of bonds significantly reduces reliability, are subject to inductive cross talk at high frequencies, and increase the cost of fabrication. Clearly, a monolithic batch-processed relatively inexpensive structure is desired.

In monolithic form, a solid-state programmable filter must accommodate acoustic surface-wave generation and detection as well as electronic switching and logic circuits on the same substrate. One approach reviewed incorporates acoustic detection and electronic switching into a single three-terminal transistor coupled to conventional logic circuitry. Piezoresistive or piezoelectric FET's may be utilized and each has its particular characteristics. A second approach extends the hybrid diode-switching technique to monolithic form through the use of thin films of silicon and a suitable piezoelectric material on a common substrate, e.g., sapphire. The SOS approach involves such problems as epitaxial growth and material compatability. However, as the technology improves, this type of device will offer significant advantages over bulk silicon substrates.

Although the preceding techniques have demonstrated capabilities, as yet there is still a need for a programmable matched filter with characteristics such as chip rates greater than 10 MHz, chip sequences greater than 100, high reliability monolithic structures, and a cost comparable with digital integrated circuits. With few exceptions, the devices available are costly, require complex fabrication procedures, cannot process long codes, and are not reliable.

Fundamentally, the integration of surface acoustic wave

and solid-state technologies is limited by fabrication yield. As an electronic device, the programmable surface-wave filter is a large-scale integration (LSI). At present only medium-scale integration (MSI) has been routinely available. In the future, two trends should take place: 1) acoustic surface-wave circuits will be compressed, and 2) LSI techniques will be improved. The former may be anticipated in the form of acoustic guided wave structures integrated into MSI chips and a gradual evolution to the LSI chip.

In conclusion, programmable matched acoustic surface-wave filters can be fabricated in either hybrid or monolithic form. At present, these devices are limited to low chip rates, short chip sequences, and frequencies in the VHF range. Extending their prerformance beyond these limits will require the integration of acoustic and electronic functions into a monolithic package. Presently the characteristics of such devices are encouraging; however, a considerable amount of development is anticipated before LSI programmable filters are available.

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